IN THE CLAIMS:

1-20.   (cancelled)

21.   (currently amended)

A method of operating a graphics system having a sequence of at least two discrete performance levels where each performance level is defined by a core clock rate of a graphics processing unit and a memory clock rate, the performance levels including a high performance level for processing complex three-dimensional graphical images and at least one lower power, lower performance level for processing less complex graphical images, the method comprising:

monitoring a single graphics pipeline in a graphics processor core clock domain, the single graphics pipeline having a set of stages in which graphics data is processed in a pipelined sequence through each subsequent stage in the graphics pipeline and detecting as a function of time a percentage of clock cycles for which a downstream stage of the graphics pipeline is held up waiting for data inputs from an upstream stage of the graphics pipeline as an indicator of utilization and determining whether the graphics pipeline is under-utilized or over-utilized, wherein the downstream stage and the upstream stage of the graphics pipeline both operate in accordance with a ~~the~~ clock rate in the graphics processor core clock domain;

in response to detecting a level of utilization greater than a non-zero, over-utilization threshold percentage level for which a display rate of the graphics system is likely to be significantly decreased below a normal display rate, selecting a higher performance level to increase the clock rate in the graphics processor core clock domain;

in response to detecting a level of utilization below a non-zero, under-utilization threshold percentage level, selecting a lower performance level to reduce the clock rate in the graphics processor core clock domain to reduce power required by the graphics system; and

operating the graphics system at the core clock rate and memory clock rate associated with the selected performance level, the selected performance level being a minimum performance level sufficient to maintain the display rate within the normal range.

22-24. (cancelled)

25. (currently amended)

A graphics system, comprising:

a graphics processor having a graphics pipeline in a graphics processor core clock domain, the graphics pipeline having a set of stages in which graphics data is processed in a pipelined sequence through each subsequent stage in the graphics pipeline, the graphics processor having a sequence of at least two discrete performance levels where each performance level is defined by a graphics processor core clock rate of the graphics processor and a memory clock rate;

a graphics memory coupled to said graphics processor by a graphics bus and operable at said memory clock rate;

a performance level controller, said performance level controller configured to monitor[[,]] as function of time a percentage of clock cycles for which a downstream stage of the graphics pipeline is held up waiting for data inputs from an upstream stage of the graphics pipeline as an indicator of utilization and determining whether the graphics pipeline is under-utilized or over-utilized, wherein the downstream stage and the upstream stage of the graphics pipeline both operate in accordance with a ~~the~~ clock rate in the graphics processor core clock domain; and

in response to detecting a level of utilization greater than an upper bound corresponding to a non-zero, over-utilization threshold percentage level, said performance level controller configured to increase said performance level to increase the clock rate in the graphics processor core clock domain to avoid over-utilization of said graphics pipeline;

in response to detecting a level of utilization below a lower bound corresponding to a non-zero, under-utilization threshold percentage level, said performance level controller configured to decrease said performance level from a high performance level to a lower performance level to decrease the clock rate in the graphics processor core clock domain to avoid under-utilization of said graphics pipeline;

the graphics system operating at the core clock rate and memory clock rate associated with the performance level selected by the performance level controller, the selected

performance level being a minimum performance level capable of maintaining the display rate within a normal range.

26-28. (cancelled)

29.   (previously presented)

    The method of claim 21, wherein said at least two discrete performance levels include a low power two-dimensional graphics performance level, a standard two-dimensional graphics performance level, a low power three-dimensional graphics performance level, and a high performance three-dimensional graphics performance level.

30.   (previously presented)

    The graphics system of claim 25, wherein the performance levels include a low power two-dimensional graphics performance level, a standard two-dimensional graphics performance level, a low power three-dimensional graphics performance level, and a high performance three-dimensional graphics performance level.

31.   (previously presented)

    The method of claim 21, wherein the non-zero, over-utilization threshold percentage level is different from the non-zero, under-utilization threshold percentage level.

32.   (new)

    The graphics system of claim 25, wherein the upper bound is different from the lower bound.